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L2: Entry 2 of 31 File: USPT Sep 23, 2003

DOCUMENT-IDENTIFIER: US 6625727 B1
TITLE: Apparatus and method for configuring a data processing system by retrieving a configuration value from storage device using reset vector and configuring parameters after reset

Detailed Description Text (3):
In another embodiment, a configuration value is fetched prior to the retrieval of the reset vector from memory. The configuration value that is fetched may include information such as the bit width (data field size) of the memory structure, information regarding the access time (wait state control information) corresponding to the memory configuration, or the byte ordering (little or big endian) used in the memory configuration. As such, the configuration value retrieved can be utilized to configure parameters that control the subsequent fetching of the reset vector from memory such that storage of the reset vector in the memory structure can be optimized to suit the type of memory utilized. In other embodiments, the configuration value retrieved may be used to configure parameters that enable/disable debug or emulation features included in the data processing system.

Detailed Description Text (35):
At step 516, those data portions of the configuration value that are to be unconditionally applied to their respective parameters are used to update those respective parameters. Thus, the former values stored at these parameters based on the initialization state are overridden by the values included in the unconditionally applied data portions of the configuration value. For example, if the hardware were initially configured to interact with an external 16-bit wide memory structure, the reset vector that is fetched at step 508 may include a configuration value that reconfigures this particular parameter to reflect that a 32-bit memory is in fact being utilized.

Detailed Description Text (44):
FIG. 7 illustrates a block diagram that reflects the use of a configuration value to configure various parameters included in the data processing system. The configuration value 710 is shown as a stand-alone value that may be unrelated to the reset vector, which is not the case with the configuration value 310 of FIG. 3. Thus, the configuration value 710 can be fetched from memory prior to fetching the reset vector for the processing system.

WEST Search History

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DATE: Friday, April 09, 2004

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☐	L1	fetch$ near5 configur$ near5 memory	125

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L2: Entry 9 of 31 File: USPT Jun 1, 1999

DOCUMENT-IDENTIFIER: US 5909557 A
TITLE: Integrated circuit with programmable bus configuration

CLAIMS:

1. An integrated circuit comprising a processor and a given number of terminals which may be configured for communicating with a selected type of external bus,

characterized in that said integrated circuit further comprises a bus controller for supplying an initial address to an external memory over said external bus during a bus configuration period, and fetching bus configuration information from said external memory over said external bus, with said fetching utilizing a fewer number of terminals than said given number, and configuring said integrated circuit so that said processor can communicate data over said external bus;

wherein said controller fetches said bus configuration information during an initial fetch that does not result in an instruction being executed by said processor.

9. An integrated circuit comprising a processor and a given number of terminals which may be configured for communicating with a selected type of external bus,

characterized in that said integrated circuit further comprises a bus controller for supplying an initial address to an external memory over said external bus during a bus configuration period, and fetching bus configuration information from said external memory over said external bus, with said fetching utilizing a fewer number of terminals than said given number, and configuring said integrated circuit so that said processor can communicate data over said external bus;

wherein said controller fetches said bus configuration information during an initial fetch that also fetches an instruction word that is executed by said processor.

17. A method of configuring an integrated circuit comprising a processor and a given number of terminals which may be configured for communicating with a selected type of external bus,

characterized by supplying an initial address to an external memory over said external bus and fetching bus configuration information from said external memory over said external bus during a bus configuration period, with said fetching utilizing a fewer number of terminals than said given number, and configuring said integrated circuit so that said processor can communicate data over said bus;

wherein said fetching fetches said bus configuration information during an initial fetch that does not result in an instruction being executed by said processor.

25. A method of configuring an integrated circuit comprising a processor and a given number of terminals which may be configured for communicating with a selected type of external bus, characterized by supplying an initial address to an external memory over said external bus and fetching bus configuration information from said

external memory over said external bus during a bus configuration period, with said fetching utilizing a fewer number of terminals than said given number, and configuring said integrated circuit so that said processor can communicate data over said bus;

wherein said fetching fetches said bus configuration information during an initial fetch that also fetches an instruction word that is executed by said processor.